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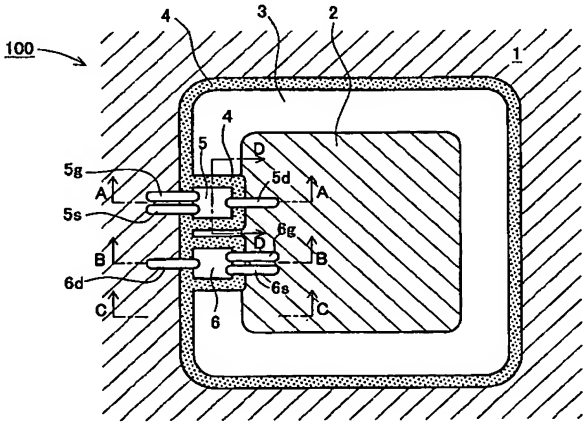

(57) Abstract: A semiconductor apparatus (100) comprises a low potential reference circuit region (1) and a high potential reference circuit region (2), and the high potential reference circuit region (2) is surrounded by a high withstand voltage separating region (3). By a trench (4) formed in the outer periphery of the high withstand voltage separating region (3), the low potential reference circuit region (1) and high potential reference circuit region (2) are separated from each other. Further, the trench (4) is filled up with an insulating material, and insulates the low potential reference circuit region (1) and high potential reference circuit region (2). The high withstand voltage separating region (3) is partitioned by the trench (4), high withstand voltage NMOS (5) or high withstand voltage PMOS (6) is provided in the partitioned position.

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